SiT92313

8 Output DB800Z Equivalent with 85 / 100 Ω Terminations

Description

The SiT92313 is a HCSL-LP, HCSL Low-Power (HCSL-LP), 8 output differential Fan-Out buffer that meets or exceed all the performance requirements of the Intel DB800Z specification. It is suitable for PCI-Express Gen1–7 or QPI/UPI applications.

The SMBus interface and multiple output-enable pins allow the configuration and control of all 8 outputs individually.

It is packaged in a compact LGA package and uses a standard pin configuration.

Applications

- Micro server and Tower server
- Rack server
- Storage area network and host bus adapter card
- Network attached storage
- Hardware accelerator

Features

- HCSL-LP outputs with Zo = 85 Ω or 100 Ω
- Saves power and board space; no termination resistors required.
- Supports PCIe and QPI applications
- Spread spectrum compatible; tracks spreading input clock for low EMI.
- Additive phase jitter.
  - Fclk=156.25 MHz (12k-20M) band ~37fs (Typical)
  - Fclk=100 MHz after PCIE Gen5 (CC) filter ~13 fs RMS
  - Fclk=100 MHz after PCIE Gen6 filter (CC) ~8 fs RMS
  - Fclk=100 MHz after PCIE Gen7 filter (CC) ~6 fs RMS
- Additive phase jitter with DB2000Q filter ~ 10 fs RMS (typical)
- Programmable output slew rate control
- Selectable SMBus address
- Output to Output Skew < 50 ps
- 3.3 V core and IO supply voltages
- Hardware-controlled low power mode (PDN)
- Current consumption: 62 mA Typical with all 8 outputs enabled at 100 MHz, driving a 10-inch T line and 2 pF load on each output.

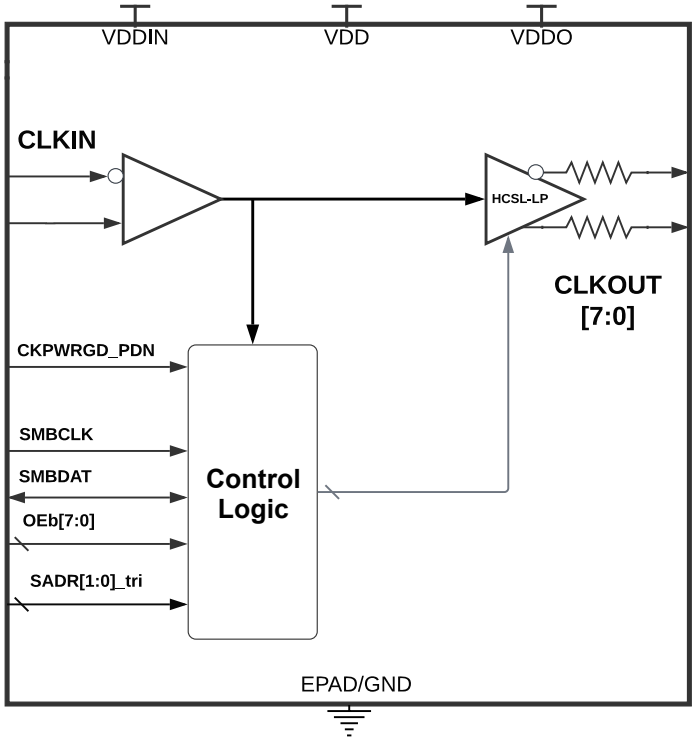


Figure 1. SiT92313 Functional Overview

Table of Contents

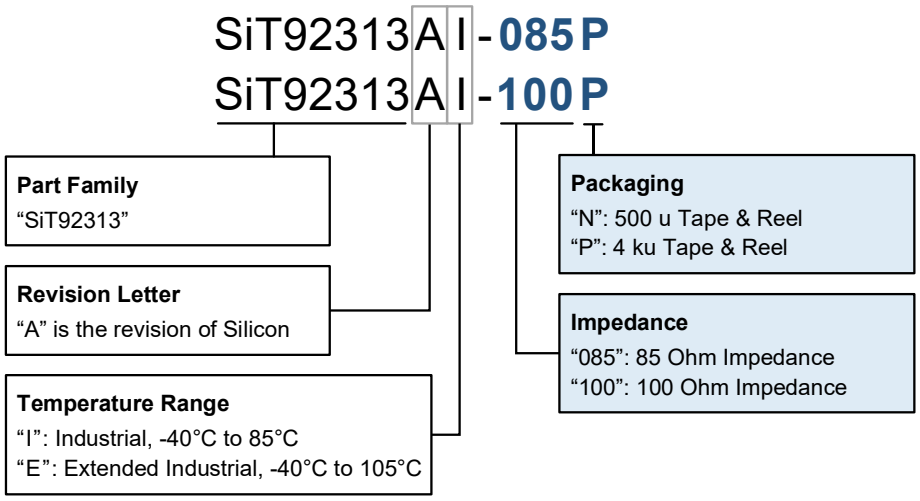
Description 1
Applications 1
Features 1
Ordering Information 3
Electrical Characteristics 4
Pin Configuration 8
Functional Description 10
- Typical Application 10
- Parameter Measurement Information 10
- Output Enable Control 11
- Using OEb Pins 11
- Using SMBus OE_CTRL bits 12
- Differential CLKIN Configurations 14
- Power Good Assertion and De-assertion 15
- Power Good De-Assertion 15
- Power Good Assertion 16
- Loss of Signal and Automatic Clock Parking 17

Serial Interface Information: SMBus 18
- Generic SMBus Description 18
- SMBus Byte: Read and Write Operations 19
- Byte Read 19
- Byte Write 19
- SMBus Block: Read and Write Operations 20
- Block Read 20
- Block Write 21
- SMBus Address Selection 22

Register Address 23
Package Dimensions and Patterns 28
- Land Pattern and Solder 29
- Top Marking 30

Revision History 31

Ordering Information



Electrical Characteristics

Table 1. Absolute Maximum Ratings

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Supply Voltage	Input Supply	VDDIN			3.63	V
Output Bank Supply Voltage	Core and Output Driver Supply	VDDO			3.63	V
Input Low Voltage		V_{IL}	GND-0.5			V
Input High Voltage		V_{IHSMB}			3.6	V
Storage Temperature		Ts	-65		150	°C
Junction Temperature		T_J			125	°C
ESD (Human Body Model)	JESD22A-114	ESD_{HBM}			2000	V
ESD (Charge Device Model)		ESD_{CDM}			500	V
Latch Up	JEDEC JESD78D	LU			100	mA
Moisture Sensitivity level		MSL		3		

Notes:

1. Exceeding maximum ratings may shorten the useful life of the device.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

Table 2. Recommended Operating Supply and Temperature

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Supply Voltage		VDDIN	2.97	3.3	3.465	V
Core Supply Voltage		VDD	2.97	3.3	3.465	V
Output Supply Voltage		VDDO	2.97	3.3	3.465	V
Ambient Temperature	Industrial (I)	T_A	-40		85	°C
	Extended industrial (E)		-40		105	°C
Junction Temperature		T_J			125	°C

Table 3. Electrical Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Operating Supply Current, CKPWRGD High[1,2]	Input Supply Current, No Clock	IDD_{VDDIN_STATIC}		8	9.5	mA
	Input Supply Current, 100 MHz Clock	IDD_{VDDIN_DYN}		7.5	9.5	mA
	Core Supply Current, No Clock	IDD_{VDD_STATIC}		13	26	mA
	Core Supply Current, 100M Clock (Industrial (I))	IDD_{VDD_DYN}		14	30	mA
	(Extended industrial (E))			14	37	mA
Output Supply Current, CKPWRGD High[1]	Output Supply Current, No Clock	IDD_{VDDO_STATIC}		17	19	mA
	All Outputs Enabled, driving a 10in T-line terminated with 2 pF cap at 100 MHz clock, SiT92313AIP	IDD_{VDDO_DYN}		62	81	mA
	SiT92313AI100P			60	79	
Power Down Current[1,2]	CKPWRGD = Low	IDD_{VDDIN_PDN}		0.001	2	mA
		IDD_{VDD_PDN}		3.35	6.5	mA
		IDD_{VDDO_PDN}		1.07	2	mA
Input Control Pin Characteristics						
Input High Voltage – logic inputs		V_{IH}	0.7 × V_{DD}			V
Input Low Voltage – logic inputs		V_{IL}			0.3 × V_{DD}	V
Input High Voltage, tri level Inputs		$V_{IH,\ TRILVL}$	0.75 x V_{DD}		V_{DD}	V

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Mid Voltage, tri level Inputs		$V_{IM, TRILVL}$	0.4 x V_{DD}	0.5 x V_{DD}	0.56 x V_{DD}	V
Input Low Voltage, tri level Inputs		$V_{IL, TRILVL}$	0		0.25 x V_{DD}	V
Pin Inductance[3]		L_{PIN}			7	nH
Capacitance[3]	Logic inputs, except CLKIN.	C_{IN}			4.5	pF
	CLKIN differential clock inputs	C_{INDIF_IN}			2.7	
	Output pin capacitance	C_{OUT}			4.5	

Notes:

1. Guaranteed by characterization.
1. Guaranteed by production testing.
2. Guaranteed by design.

Table 4. Input Clock Characteristics

Unless otherwise specified: VDDIN = 3.3 V ±5%, VDDO = 3.3 V ±5%, -40°C ≤ TA ≤ 105°C, CLKin driven differentially.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input frequency range		F_{CLKin}	1		400M	Hz
Peak differential input voltage swing		VID	0.1			V
Input Slew Rate – CLK_{IN}	Measured differentially	dv/dt	0.2		4	V/ns
Input Leakage Current	VIN = VDD, VIN = GND	I_{IN}	-5		5	uA
Input Duty Cycle	Measurement from differential waveform	dtin		50		%
Input Crossover Voltage	Crossover voltage		0.1		0.9	V

Notes:

1. Additive jitter performance depends on the input slew rate. Higher input slew rate often will result in lower additive jitter.

Table 5. Output Clock Characteristics (HCSL-LP) at 100 MHz

$T_A = T_{COM}$; Supply Voltage VDDO = 3.3 V ±5%

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Slew rate[1,5]	Scope averaging on	T_{rf}	2.3	2.9	3.5	V/ns
Slew rate matching[1]	Slew rate matching, Scope averaging on	ΔT_{rf}			20	%
Voltage High[1,5]	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	V_{High}	750	801	843	mV
	(Extended industrial (E))		745.5	800.8	843.2	mV
Voltage Low[1]		V_{Low}	-166	9	155	mV
Max Voltage[1,5]	Measurement on single ended signal using absolute value. (Scope averaging off)	V_{max}	788	838	877	mV
Min Voltage[1]		V_{min}	-148	-26	57	
	(Extended industrial (E))	V_{min}	-147.60	-26	57	mV
Vswing[1,5]	Scope averaging off [pk to pk, single ended]	V_{SWING}	800	864	942	mV
Crossing Voltage (abs)[1]	Scope averaging off	V_{cross_abs}	346	412	466	mV
Crossing Voltage (var)[1]	Scope averaging off	Δ-Vcross	-20	31.5	83	mV
Differential Impedance[2]	SiT92313AIP	Z_{DIFF}	80	85	90	Ω
	SiT92313AI100P		94	100	106	Ω
Clock Stabilization[3,4]	From VDDO power-up and after input clock stabilization or assertion of CKPWRGD to 1st Clock	T_{STABLE}		1.0	1.8	ms
OEb Latency[3,4]	DIF starts after OEb assertion DIF stop after OEb de-assertion	t_{LATOEb}	4		6	Clocks

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Tdrive_PDb[3,4]	DIF output enable after CKPWRGD assertion	t_{DRVPDb}		100	300	µs

Notes:

1. Guaranteed by characterization.
2. Guaranteed by production testing.
3. Control input must be monotonic from 20 % to 80 % of input swing.
4. Guaranteed by limited testing of typical parts.
5. The cpk=1.33.

Table 6. SMBus Electrical Parameters

$T_A = T_{AMB}$. Supply voltages are per normal conditions. See Test loads for loading conditions.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
SMBus Input Low Voltage[1]		V_{ILSMB}			0.3 x VDD	V
SMBus Input High Voltage[1]		V_{IHSMB}	0.7 x VDD		VDD	V
Hysteresis on SMBUS pins		V_{HYS}	0.048			V
SMBus Output Voltage[1]	I_{OH} = -2 mA	V_{OHSMB}	0.75 x VDD			V
	I_{OL} = 2 mA	V_{OLSMB}			0.25 x VDD	V
SMBus Operating Frequency[1]		f_{SMB}	4		400	kHz
Max Capacitive Load for Each Bus line		C_B		400		pf

Table 7. Skew and Differential Jitter Parameters

Parameter	Conditions	Symbol	Min	Typ	Max	Units
CLKINx, CLKOUTx[1,2,4,5,6,7]	Input-to-Output delay in nominal value @ 25 °C, 3.3 V (Industrial (I))	t_{PD}	566	764	949	ps
	(Extended industrial (E))		537		988	ps
CLKINx, CLKOUTx [1,2,6,7,8]	Input-to-Output delay Variation across temperature	t_{PD_DRIFT}			1.2	ps/°C
DIF[2,5,6,7,9]	Output-to-Output delay across all outputs (Industrial (I))	t_{SKEW_ALL}			50	ps
	(Extended industrial (E))				55	ps
DIF Skew	Output to output skew variation across temp				0.2	ps/ºC
Duty Cycle Distortion [3,5,6]	Measured differentially, @100 MHz	t_{DCD}	-1.3	0.1	1	%

Notes:

1. Guaranteed by design and characterization, not 100 % tested in production.
2. Differential cross-point to differential cross-point measurement.
3. The difference in Duty Cycle between the output and input clock is referred as Duty Cycle Distortion
4. Mean Value measured through scope averaging.
5. Measured from differential waveform.
6. Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
7. All input-to-output specs refer to the timing between an input edge and the specific output edge created by it.
8. This is the amount of input-to-output delay variation with respect to temperature.

Table 8. PCIe Phase Jitter Parameters with 100 MHz Clock

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Additive Phase Jitter Common Clock	PCIe Gen 1 HF [1,2,3,4]	$tjph_{PCIeG1-CC}$		1.9	4.7	ps (p-p)
	PCIe Gen 2 HF [1,2,3,4,5,6]	$tjph_{PCIeG2-CC}$		102	138.4	fs rms
	PCIe Gen 2 LF [1,2,3,4,5,6]	$tjph_{PCIeG2-CC}$		4	7.7	fs rms
	PCIe Gen 3[1,2,3,4,5,6]	$tjph_{PCIeG3-CC}$		33	44.3	fs rms
	PCIe Gen4[1,2,3,4,5,6]	$tjph_{PCIeG4-CC}$		33	44.3	fs rms
	PCIe Gen5[1,2,3,4,5,6]	$tjph_{PCIeG5-CC}$		13	17.5	fs rms
	PCIe Gen6[1,2,3,4,5,6]	$tjph_{PCIeG6-CC}$		8	10.6	fs rms
	PCIe Gen7[1,2,3,4,5,6]	$tjph_{PCIeG7-CC}$		5	7.4	fs rms
Additive Phase Jitter SRIS	PCIe Gen 2 HF [1,2,3,45,6]	$tjph_{PCIeG2-SRIS}$		70	122.7	fs rms
	PCIe Gen 2 LF [1,2,3,4,5,6]	$tjph_{PCIeG2-SRIS}$		18	2.8	fs rms
	PCIe Gen 3[1,2,3,4,5,6]	$tjph_{PCIeG3-SRIS}$		29	53.7	fs rms
	PCIe Gen4[1,2,3,4,5,6]	$tjph_{PCIeG4-SRIS}$		30	55.3	fs rms
	PCIe Gen5[1,2,3,4,5,6]	$tjph_{PCIeG5-SRIS}$		10	17.1	fs rms
	PCIe Gen6[1,2,3,4,5,6]	$tjph_{PCIeG6-SRIS}$		7	11	fs rms
	PCIe Gen7[1,2,3,4,5,6]	$tjph_{PCIeG7-SRIS}$		4	8.7	fs rms
Additive Phase Jitter SRNS	PCIe Gen 2 HF [1,2,3,4,5,6]	$tjph_{PCIeG2-SRNS}$		68	110	fs rms
	PCIe Gen 2 LF [1,2,3,4,5,6]	$tjph_{PCIeG2-SRNS}$		1	1.3	fs rms
	PCIe Gen 3[1,2,3,4,5,6]	$tjph_{PCIeG3-SRNS}$		24	36.2	fs rms
	PCIe Gen4[1,2,3,4,5,6]	$tjph_{PCIeG4-SRNS}$		24	36.2	fs rms
	PCIe Gen5[1,2,3,4,5,6]	$tjph_{PCIeG5-SRNS}$		9	13.2	fs rms
	PCIe Gen6[1,2,3,4,5,6]	$tjph_{PCIeG6-SRNS}$		6	9.7	fs rms
	PCIe Gen7[1,2,3,4,5,6]	$tjph_{PCIeG7-SRNS}$		4	6.8	fs rms

Notes:

1. Applies to all the differential outputs, guaranteed by design and characterization.
2. Applies to all the outputs when driven by a low phase noise source SMA100B.
3. Additive RMS Jitter measurements were made by capturing 100,000 clock cycles using real time oscilloscope with a minimum sampling rate of ≥40 GSa/s and with the waveform covering 90% of the DSO screen. All the post processing in DSO is disabled to decrease the additional jitter impact from oscilloscope. Broadband oscilloscope noise is also minimized in the measurement.
4. Alternately, jitter measurements can be done using a Phase Noise Analyzer (PNA). Since PNA stored data doesn't include the noise folded into the clock jitter by the clock edge sampling the data eye, extraction of jitter can be done after extending the flat band and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz below the Nyquist frequency.
5. Additive jitter for RMS values is calculated by solving the equation for b [b=sqrt(c^2-a^2)] where 'a' is the rms input jitter and "c" is the rms total jitter.
6. Common input conditions: Differential Input swing: 1600 mV; Differential Input slew rate: 4.8 V/ns

Table 9. Phase Jitter Parameters

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Additive Phase Jitter	Fclk = 156.25M, 12K-20MHz (Industrial (I))	tjph_12K_20M		37	45	fs rms
	Fclk = 156.25M, 12K-20MHz (Extended Industrial (E))				49	
	Fin = 312.5 MHz 12K-20MHz with 4MHz HPF (Industrial (I))	tjph_420B		20	28	fs rms
	Fin = 312.5 MHz 12K-20MHz with 4MHz HPF (Extended Industrial (E))				30	

Table 10. Thermal Characteristics of SiT92313

Thermal Metric	SiT92313	Units
θ_{JA} Junction to ambient thermal resistance, flow = 0 m/s	34.7	°C/W
θ_{JA} Junction to ambient thermal resistance, flow = 1 m/s	39.2	°C/W
θ_{JA} Junction to ambient thermal resistance, flow = 2 m/s	38.6	°C/W
θ_{JB} Junction to board	21.1	°C/W
θ_{JC} Junction to case	29.32	°C/W
ψ_{JT} Junction to top characterization parameter	16.1	°C/W

Notes:

1. Thermal characteristics of the SiT92313 is based on 4 layer 2S2P PCB, as per JEDEC standards. PCB center land with 36 vias to top internal plane on PCB.

Pin Configuration

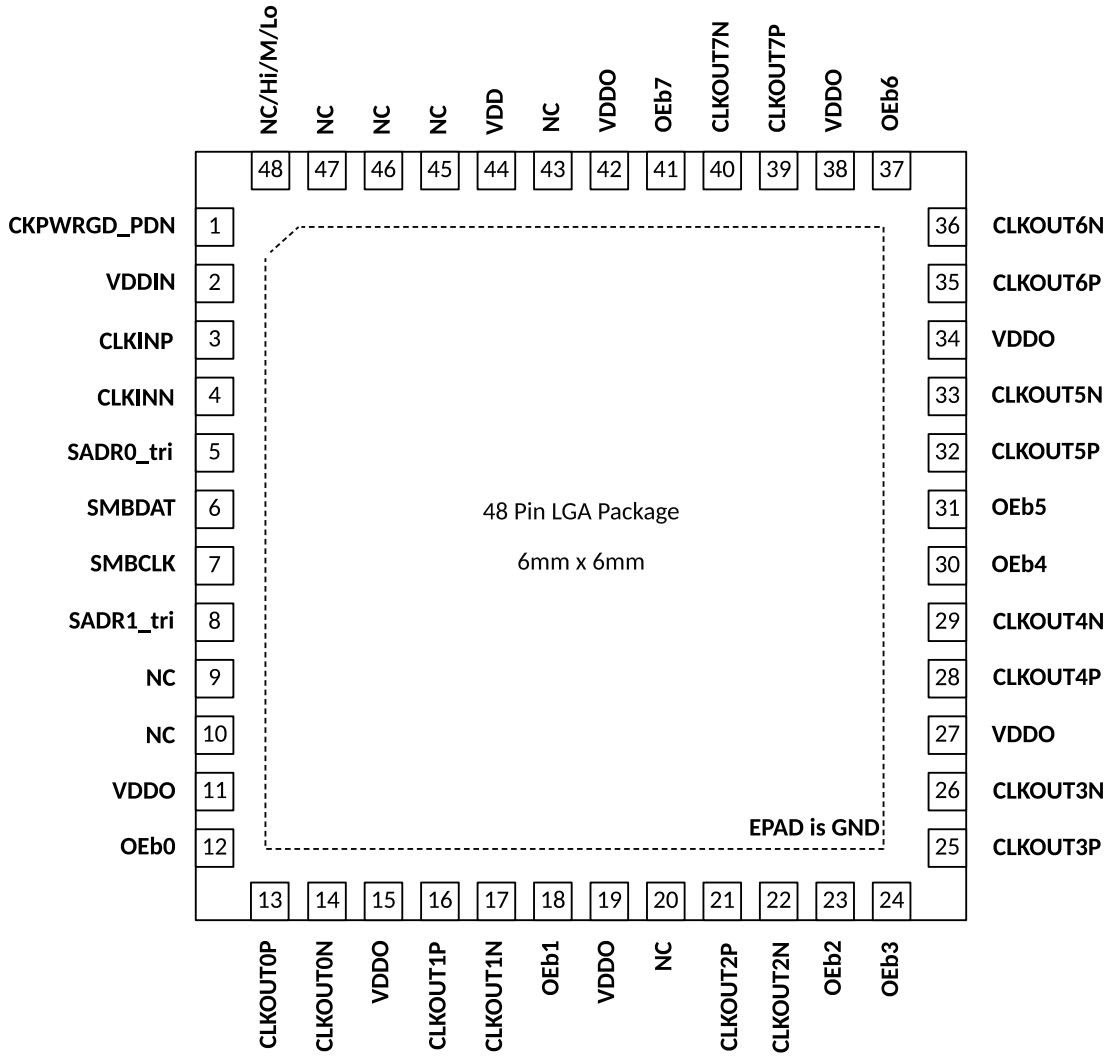


Figure 2. SiT92313 Pin Configuration

Table 11. Pin Description

Pin Name	Pin No.	I/O Type	Descriptions
CKPWRGD_PDN	1	I, PU, PDT	3.3 V Input notifies device to sample latched inputs and start up on first high assertion or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.
VDDIN	2	PWR	3.3 V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.
CLKINP	3	I,PDT	HCSL-LP Differential True input
CLKINN	4	I,PDT	HCSL-LP Differential Complementary Input
SADR0_tri	5	I, PU/PD, PDT	SMBus address strap pin. There is a 3 level input decoding on this pad
SMBDAT	6	I/O, OD, PDT	Data pin of SMBus circuitry, 3.3 V tolerant
SMBCLK	7	I, OD, PDT	Clock pin of SMBus circuitry, 3.3 V tolerant
SADR1_tri	8	I, PU/PD, PDT	SMBus address strap pin. There is a 3 level input decoding on this pad
NC/Hi/M/Lo	48	N/A	This pin does not have any specific user function. NC or any static level will be acceptable.

Pin Name	Pin No.	I/O Type	Descriptions
NC	9, 10, 20,43,45, 46,47	N/A	No Connection. Recommended to be grounded.
VDDO	11, 15, 19, 27, 34, 38, 42	PWR	Power Supply for the Output Drivers, nominal 3.3 V
OEb0	12	I, PD, PDT	Active low input for enabling Clock pair 0. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT0P	13	O	HCSL-LP differential true clock output
CLKOUT0N	14	O	HCSL-LP differential Complementary clock output
CLKOUT1P	16	O	HCSL-LP differential true clock output
CLKOUT1N	17	O	HCSL-LP differential Complementary clock output
OEb1	18	I, PD, PDT	Active low input for enabling Clock pair 1. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT2P	21	O	HCSL-LP differential true clock output
CLKOUT2N	22	O	HCSL-LP differential Complementary clock output
OEb2	23	I, PD, PDT	Active low input for enabling Clock pair 2. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
OEb3	24	I, PD, PDT	Active low input for enabling Clock pair 3. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT3P	25	O	HCSL-LP differential true clock output
CLKOUT3N	26	O	HCSL-LP differential Complementary clock output
CLKOUT4P	28	O	HCSL-LP differential true clock output
CLKOUT4N	29	O	HCSL-LP differential Complementary clock output
OEb4	30	I, PD, PDT	Active low input for enabling Clock pair 4. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
OEb5	31	I, PD, PDT	Active low input for enabling Clock pair 5. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT5P	32	O	HCSL-LP differential true clock output
CLKOUT5N	33	O	HCSL-LP differential Complementary clock output
CLKOUT6P	35	O	HCSL-LP differential true clock output
CLKOUT6N	36	O	HCSL-LP differential Complementary clock output
OEb6	37	I, PD, PDT	Active low input for enabling Clock pair 6. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
CLKOUT7P	39	O	HCSL-LP differential true clock output
CLKOUT7N	40	O	HCSL-LP differential Complementary clock output
OEb7	41	I, PD, PDT	Active low input for enabling Clock pair 7. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
VDD	44	PWR	3.3 V power for the Core Supply.

Notes:

1. PU is weak internal Pull-up with 200 KΩ resistor.
2. PD is weak internal Pull-down with 200 KΩ resistor.
3. PU/PD are weak internal Pull-up/Pull-down with 200 KΩ resistor.
4. PDT (Power Down Tolerant) pins can be driven when the device is powered down without accidentally waking up the device.
5. Clock input pins are power down tolerant for voltage level < 1.8V on pins.
6. OD (Open Drain). It requires an external Pull-up on the board.
7. Refer Table 3 for input control pin (VIH and VIL) characteristics.
8. 'b' suffix (in OEb) indicates an active-low control.

.

Functional Description

Typical Application

Figure 3 shows a SIT92313 typical application. In this application, a clock generator provides a 100-MHz reference to the SIT92313 which then distributes that clock to PCIe endpoints. The clock generator may either be a discrete clock generator, or it may be integrated in a larger component such as a Platform Controller Hub (PCH) or application processor.

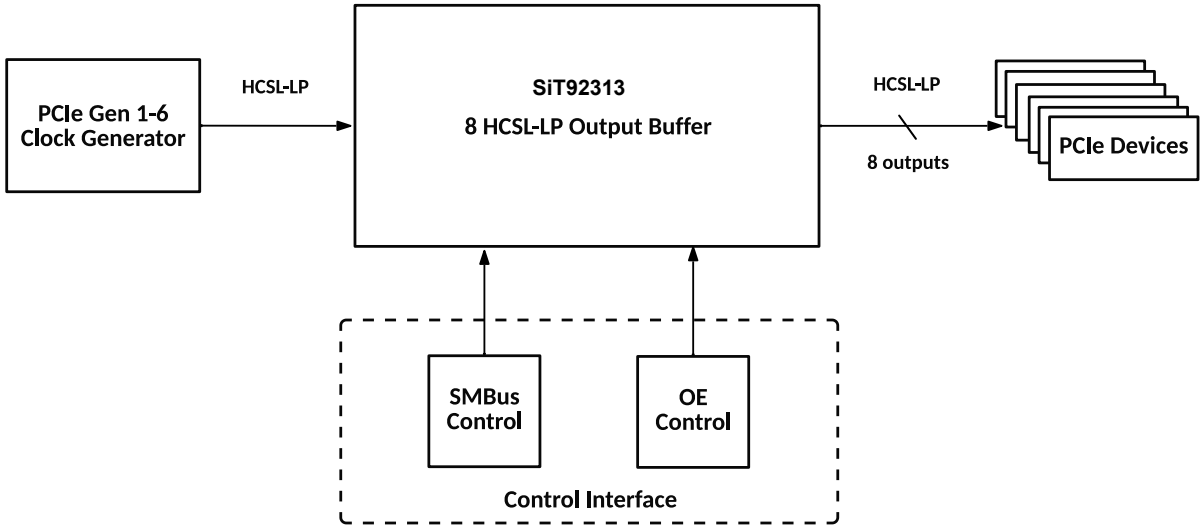


Figure 3. Typical Application Diagram

Parameter Measurement Information

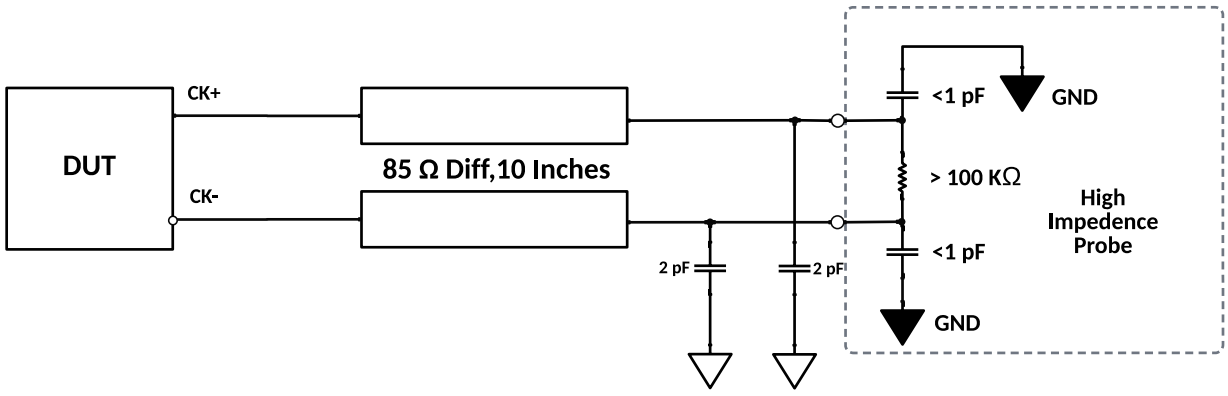


Figure 4. AC Test Mode

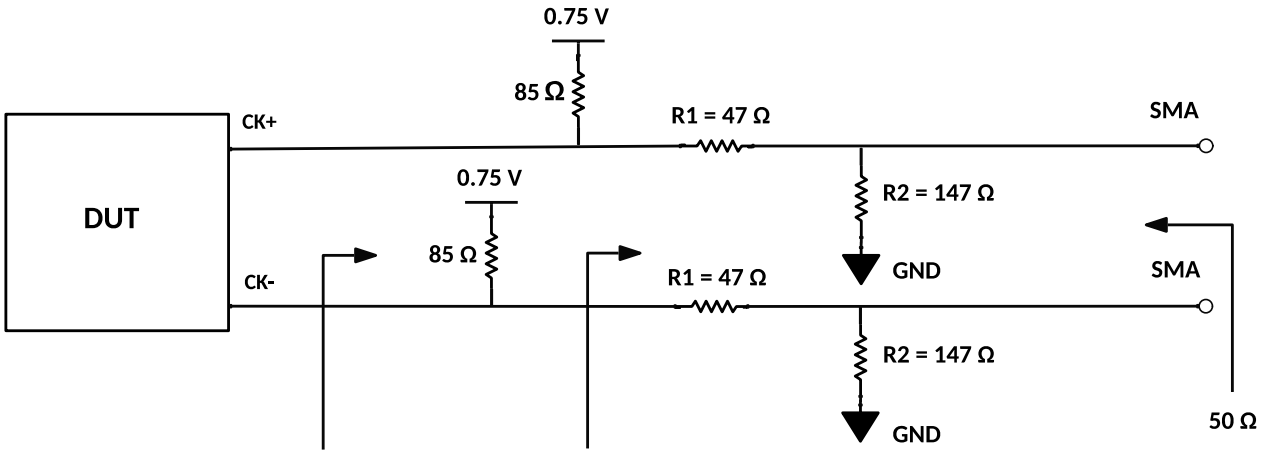


Figure 5. DC Simulation Mode

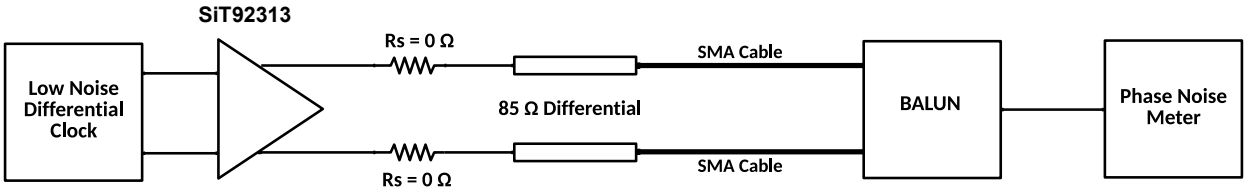


Figure 6. Phase Noise Measurement Setup

Output Enable Control

The device provides two methods to enable or disable output clocks in a glitch free manner. Output clock is enabled only when all methods indicate "enabled" condition.

Using OEb Pins

The device provides control over output clocks using OEb pins. Each OEb pin provides individual output enable control using active low input.

When OEbx is asserted (V_{IH}), corresponding CLKOUTx will be held at the states as defined in STOP_STATE_CONFIG_REG register (register 0x14) in regmap and when OEbx is de-asserted (V_{IL}), corresponding CLKOUTx will be enabled.

These OEb status can also be read back using register 0x03 in regmap.

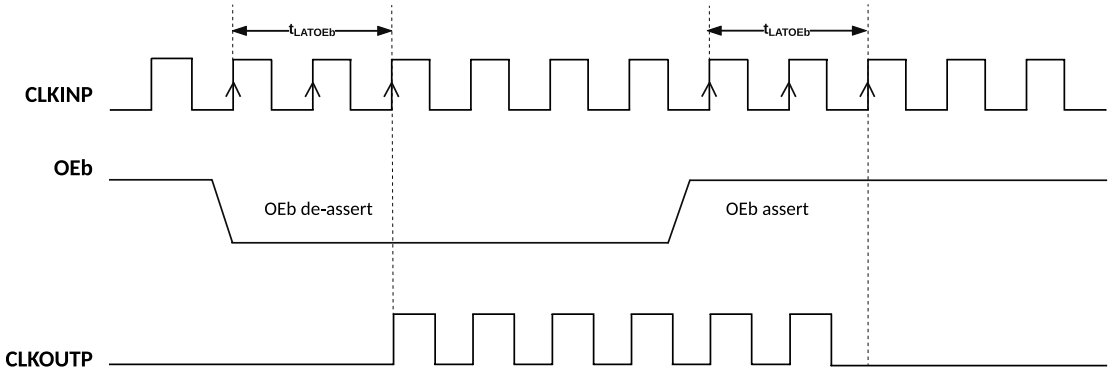


Figure 7. OEb Assert and De-assert Sequence

Table 12. OEb Map of SiT92313

OEb	Control
OEb0	CLKOUT0
OEb1	CLKOUT1
OEb2	CLKOUT2
OEb3	CLKOUT3
OEb4	CLKOUT4
OEb5	CLKOUT5
OEb6	CLKOUT6
OEb7	CLKOUT7

Using SMBus OE_CTRL bits

The device provides individual control over each output clocks using dedicated SMBus output enable control bit. A True condition (1) on the OE_CTRL bit will 'enable' and a False condition (0) on the OE_CTRL bit will 'disable' the respective CLKOUT.

Check 0x01 and 0x02 in Table 17 for OE_CTRL bits.

Since SMBus interface is active only when CKPWRGD_PDN is High (V_{IH}), registers has to be written only when CKPWRGD_PDN is High (V_{IH}).

These written contents will be retained till V_{DD} remains in operating limit. The priority of these controls is formalized.

Table 13. Input vs Output States

Control Inputs	CLKIN	OEb[7:0] HARDWARE PINS AND SMBus CONTROL REGISTER BIT			CLKOUT[7:0]_P / CLKOUT[7:0]_N
CKPWRGD_PDN		OE[7:0]b Pin	OUT_EN_CLK[7:0]	STOP_STATE_CONFIG_REG	
1	X	X	0	0	LOW/LOW
				1	HiZ/HiZ
				2	High/Low
				3	Low/High
		1	X	0	LOW/LOW
				1	HiZ/HiZ
				2	High/Low
				3	Low/High
	Running	0	1	X	Output Follow input
0	X	X	X	0	LOW/LOW

The device provides selection of P and N states of the CLKOUT when they are STOPPED. It can be selected using register 0x14 from regmap (refer Table 17).

Table 14. Stop State Configuration

STOP_STATE_CONFIG_REG[1:0]	CLKOUTP	CLKOUTN
00	LOW	LOW
01	HIZ	HIZ
10	HIGH	LOW
11	LOW	HIGH

Note:

1. Stop State bits are mentioned in binary.

Differential CLKIN Configurations

The SiT92313 clock input buffer supports four configurations:

- Direct connection to HCSL-level inputs.
- Direct connection to LVDS-level inputs with external termination resistor.
- Internal self-bias circuit for applications that externally AC-couple the input clock.
  - This feature is enabled by the AC_IN bit.
- Internal pull-down resistors (Rp) to terminate the clock input at the receiver.
  - This feature is enabled by the Rx_TERM bit.

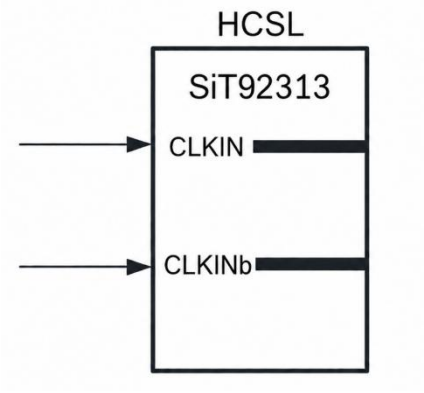


Figure 8. HCSL Input Levels (PCIe Standard)

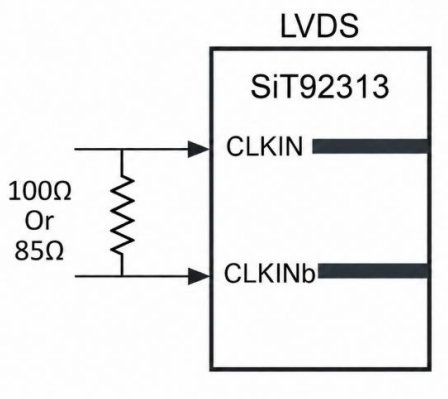


Figure 9. LVDS Input Levels

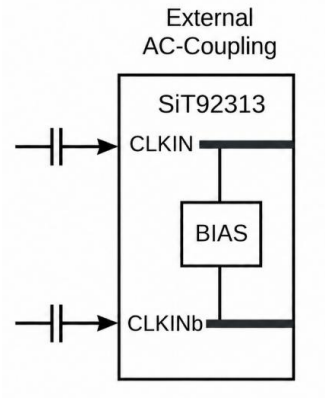


Figure 10. External AC-Coupling

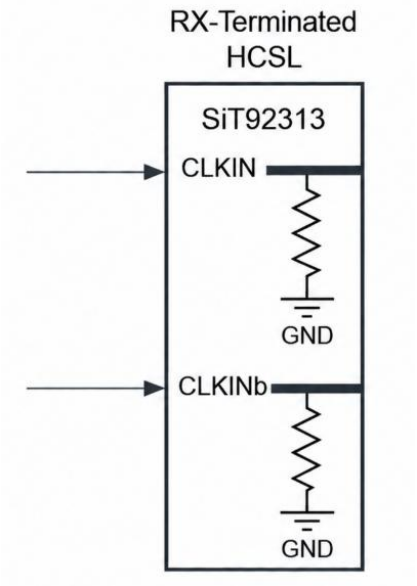


Figure 11. Receiver Termination

Power Good Assertion and De-assertion

Power Good (CKPWRGD_PDN) is asserted high and de-asserted low. De-assertion of CKPWRGD_PDN (pulling the signal low) is equivalent to indicating a powerdown condition. CKPWRGD_PDN (assertion) is used by the DB800Z to sample initial configurations such as SA selections.

After CKPWRGD_PDN has been asserted high for the first time, the pin becomes a PWRDNb (Power Down) pin that can be used to shut off all clocks cleanly and instruct the device to invoke power savings mode. PWRDNb is a completely asynchronous active low input.

When entering power savings mode, PWRDNb should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch free manner. When PWRDNb is de-asserted high, all clocks will start and stop without any abnormal behavior and will meet all AC and DC parameters.

NOTE: The assertion and de-assertion of PWRDNb is asynchronous.

Warning: Disabling of the CLKIN input clock prior to the assertion of PWRDNb is an undefined

mode and is not recommended. Operation in this mode may result in glitches.

Power Good De-Assertion

When PWRDNb is sampled low by two consecutive rising edges of CLKINN, all differential outputs must be held Tri-stated on the next CLKINN high to low transition.

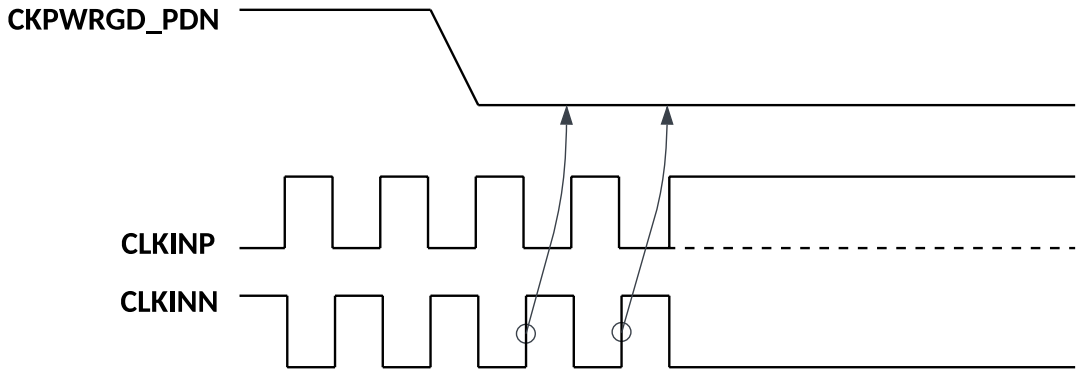


Figure 12. Power Good Assertion

Power Good Assertion

CKPWRGD_PDN must not be asserted to the clock buffer before VDD reaches VDD_{MIN}. Prior to VDD_{MIN} it is recommended to hold PWRGD low (less than 0.5 V).

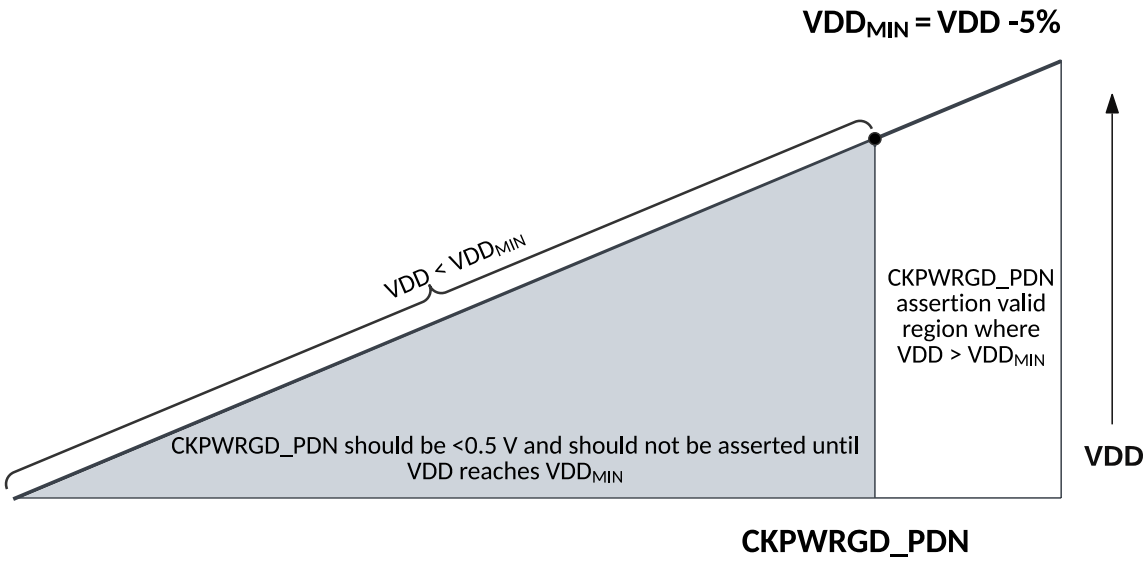


Figure 13. Power Good vs VDD3P3 relationship

This is the time from the valid CLKINx input and the assertion of the PWRGD signal until the output of the stable clocks from the buffer chip.

All differential outputs stopped in a Tri-state condition resulting from power down must be driven high in less than 300 µs of the PWRGD assertion to a voltage greater than 200 mV.

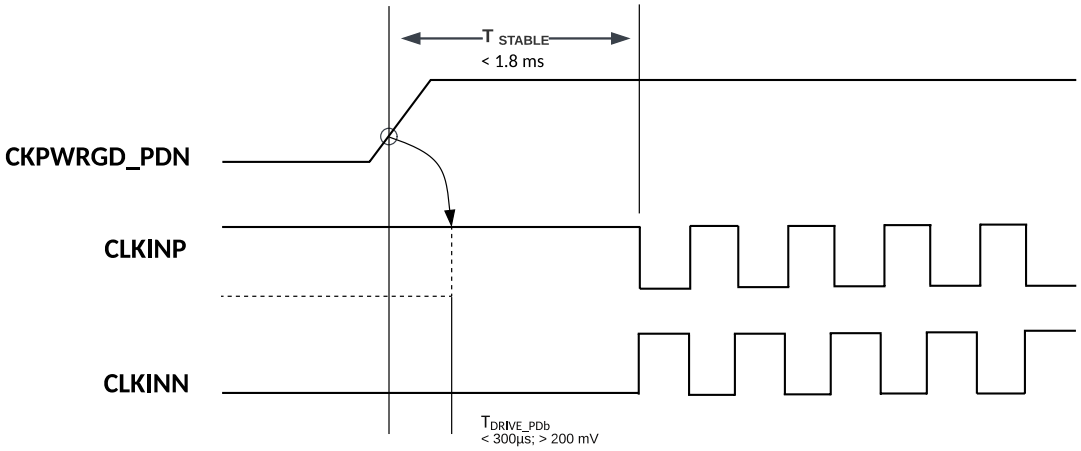


Figure 14. Power Good Assertion

Loss of Signal and Automatic Clock Parking

The SiT92313 buffer has a Loss of Signal (LOS) circuit to detect the presence or absence of an input clock. The LOS circuit drives the open-drain LOSb pin (the "b" suffix indicates "bar", or active-low) and sets the LOS_EVT bit in the SMBus register space.

Figure 15 shows the LOSb de-assertion timing for the SiT92313 output buffer. LOSb on the SiT92313 output buffer defaults to low at power up.

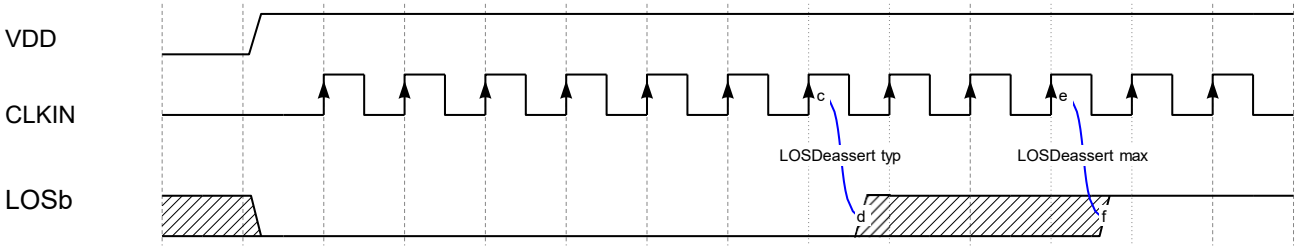


Figure 15. Loss of Signal De-assertion Timing

Figure 16 shows the LOSb assertion sequence when the CLKIN is lost. It also shows the Automatic Clock Parking (ACP) circuit bring the outputs to a Low/Low state after an LOS event.

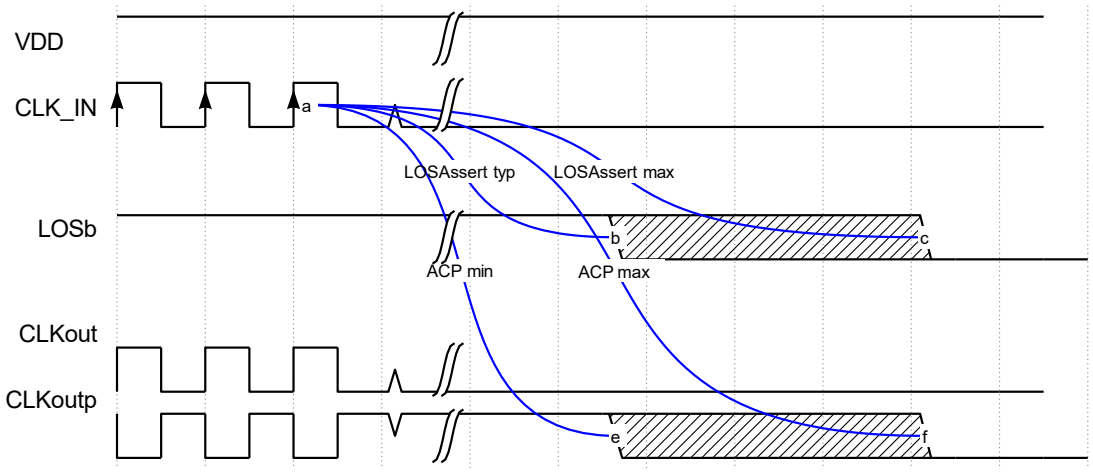


Figure 16. Loss of Signal Assertion Sequence

Serial Interface Information: SMBus

System Management Bus (SMBus) is a 2 wire interface, which uses SMBCLK and SMBDAT on the device for serial communication. SMBus will be active only when CKPWRGD_PDN is High (V_{IH}).

Generic SMBus Description

The Figure 17 illustrates a generic SMBus sequence along with the description and functions of the constituent bytes elaborated in Table 15.

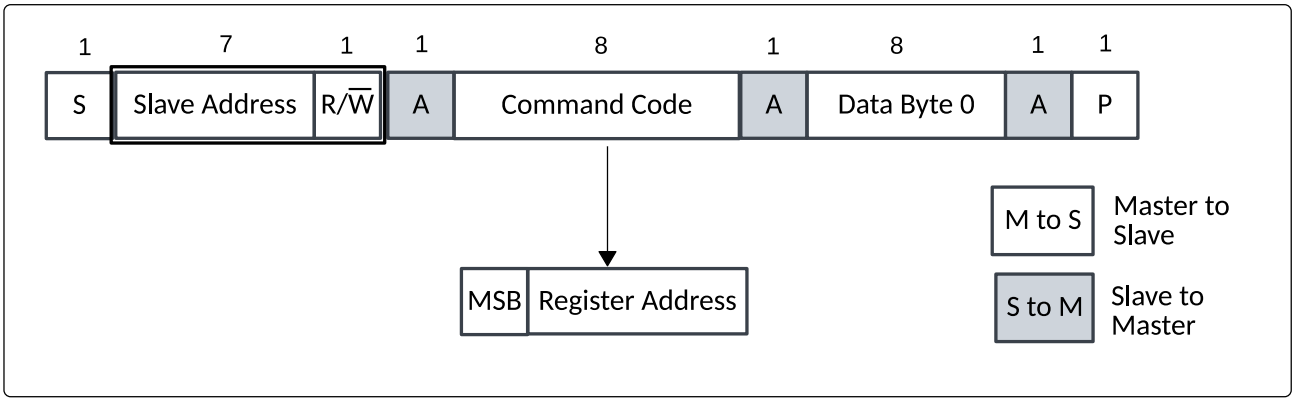


Figure 17. Generic SMBus Sequence

Table 15. SMBus Address Register Description

Description	Bit Range	Functions
S	1	Start Condition
Sr	1	Repeated start condition
Slave Address	7 [7:1]	Address of the slave device.
R/W	1 [LSB]	1 = Read (Rd), 0 = Write (Wr)
A	1	1 = No-Acknowledgement (NA), 0 = Acknowledgement (A)
P	1	Stop condition
Command Code	1 [MSB]	1 = Byte read/write, 0 = Block read/write
	7 [6:0]	Register address

The register number should be specified when reading or writing a register in a SMBus slave device. While mentioning the register address, MSB must be SET for byte operation and must be RESET for block operations.

SMBus Byte: Read and Write Operations

Byte Read

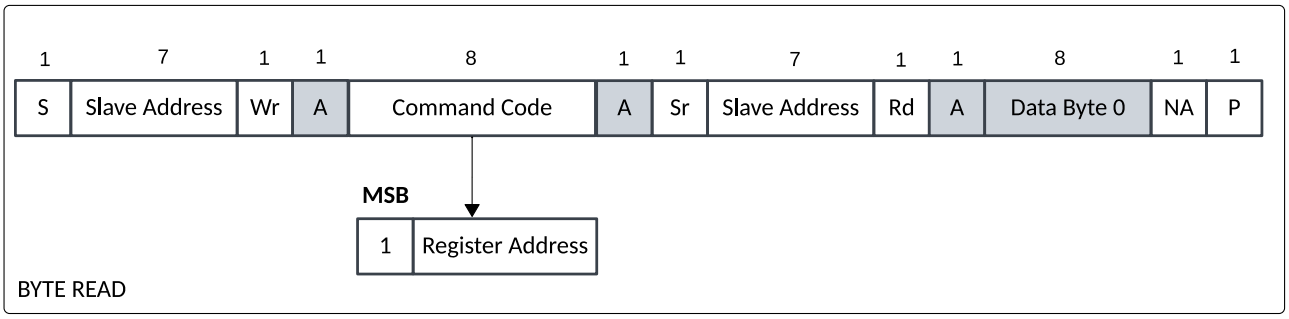


Figure 18. Byte Read Operation

- Master sends a start bit
- Master sends the slave address with LSB = Write
- Slave device will send acknowledgement (A)
- Master sends 8 bit register address (with MSB = 1 and byte read starting address [6:0])
- Slave device will send acknowledgement (A)
- Master sends a repeated start bit
- Master sends the slave address with LSB = Read
- Slave device will send acknowledgement (A)
- Slave device will send data byte
- Master will send not-acknowledgment (NA)
- Master will send a stop bit.

Byte Write

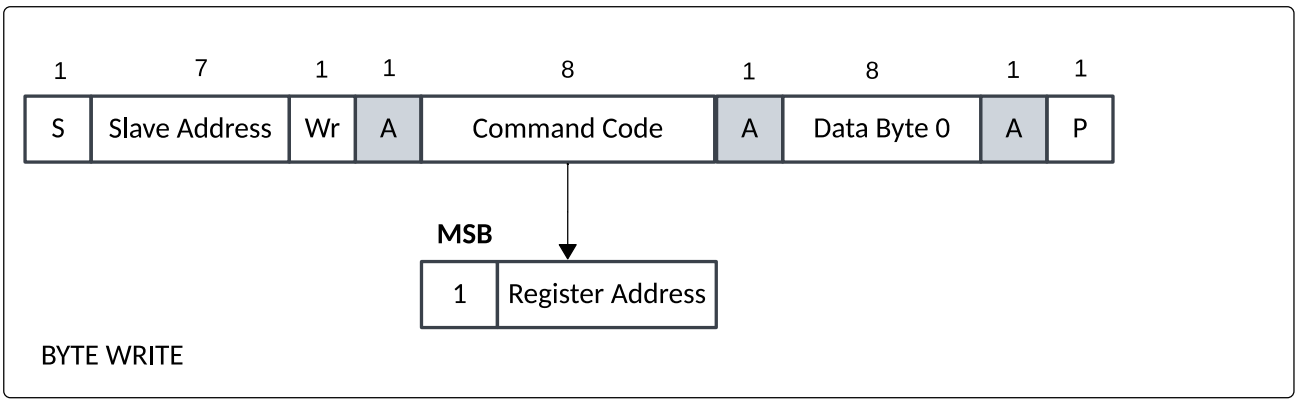


Figure 19. Byte Write Operation

- Master sends a start bit
- Master sends the slave address with LSB = Write
- Slave device will send acknowledgement (A)
- Master sends 8 bit register address (with MSB = 1 and byte write starting address [6:0])
- Slave device will send acknowledgement (A)
- Master sends data byte to be written
- Slave device will send acknowledgement (A)
- Master sends a stop bit

SMBus Block: Read and Write Operations

Block Read

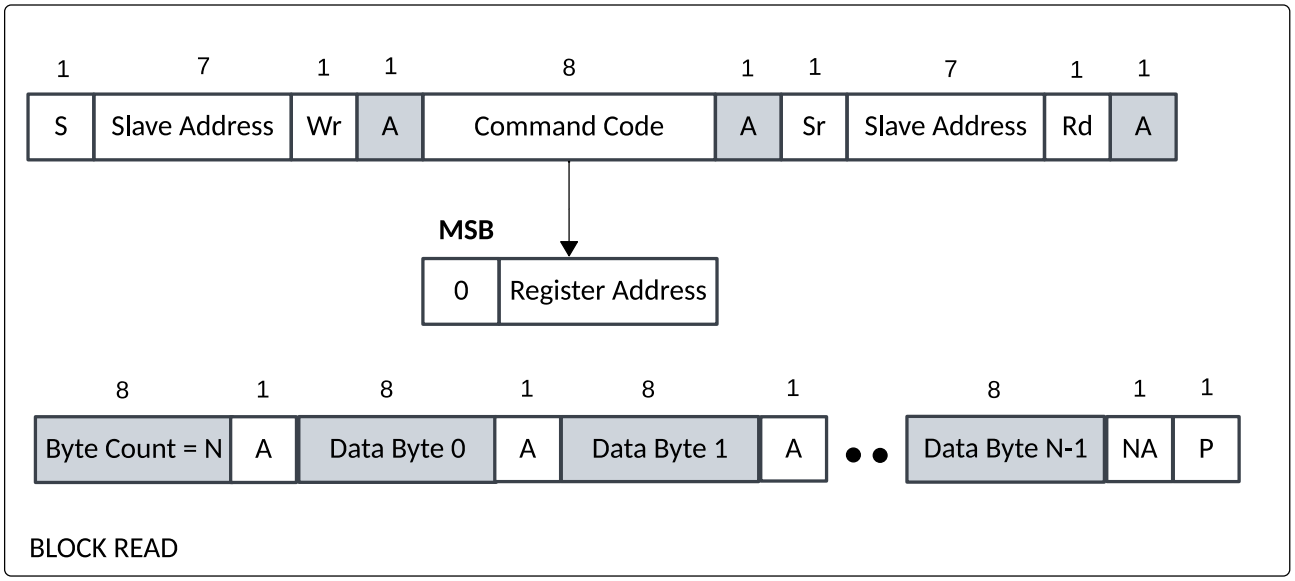


Figure 20. Block Read Operation

- Master sends a start bit
- Master sends the slave address with LSB = Write
- Slave device will send acknowledgement (A)
- Master sends 8 bit register address (with MSB = 0 and block read starting address [6:0])
- Slave device will send acknowledgement (A)
- Master sends a repeated start bit
- Master sends the slave address with LSB = Read
- Slave device will send acknowledgement (A)
- Slave device will send byte count N (0 < N < 33) that slave will transfer to the master
- Master sends acknowledgement (A)
- Slave device sends data bytes from data byte 0 to data byte N-1
- Master will send acknowledgement (A) for each data byte received (one at a time) except for the last data byte (N-1)
- Master will send not-acknowledgment (NA)
- Master will send a stop bit

Block Write

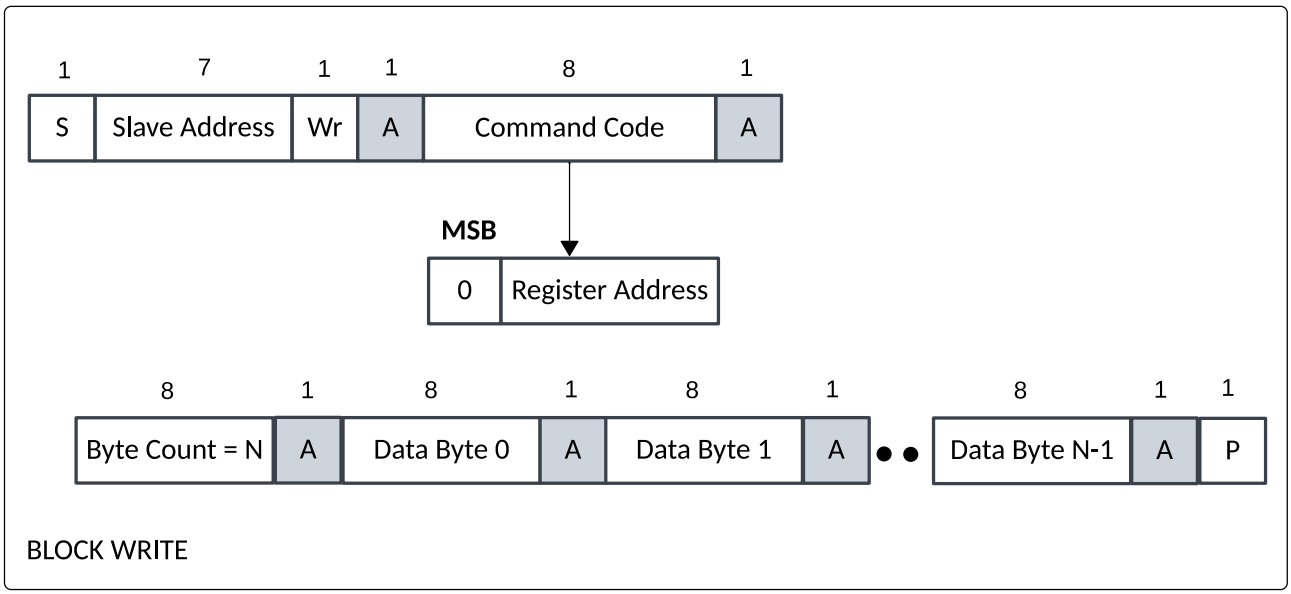


Figure 21. Block Write Operation

- Master sends a start bit
- Master sends the slave address with LSB = Write
- Slave device will send acknowledgement (A)
- Master sends 8 bit register address (with MSB = 0 and block write starting address [6:0])
- Slave device will send acknowledgement (A)
- Master sends byte count N (0 < N < 33) that master will transfer to the slave device
- Slave device will send acknowledgement (A)
- Master sends data bytes to be written from data byte 0 to data byte N-1
- Slave device will send acknowledgement (A) for each data byte received (one at a time)
- Master sends a stop bit

Note: For cases where an SMBus bus transaction concludes with a write operation, ensure that the SMBus master does not toggle the clock inadvertently between the STOP and the next START condition to prevent unintended write operations. For cases where inadvertent clocks can occur between the STOP and the next START condition, it is recommended to conclude the SMBus transaction with a read operation.

SMBus Address Selection

The SMBus address is selected by setting the SADR0_tri and SADR1_tri pins. These pins are capable of supporting three levels, which allows SiT92313 to select nine different SMBus addresses. The address can be changed by setting SMBus address pin level and power cycling the device. The SMBus address pin is sampled when CKPWRGD_PDN is set to High (V_{IH}) after the power cycle. See Table 16 for Address Pin Configuration

Table 16. SMBus Address Selection

Address Selection[3]		SMBus Address								
SADR1_tri	SADR0_tri	In Binary[1,2]								SMBUS address (excluding Bit 0)
		7	6	5	4	3	2	1	R/$\overline{W}$	
L	L	1	6C	0	1	1	0	0	0	6C
	M	1	6D	0	1	1	0	1	0	6D
	H	1	6F	0	1	1	1	1	0	6F
M	L	1	61	0	0	0	0	1	0	61
	M	1	62	0	0	0	1	0	0	62
	H	1	63	0	0	0	1	1	0	63
H	L	1	65	0	0	1	0	1	0	65
	M	1	66	0	0	1	1	0	0	66
	H	1	67	0	0	1	1	1	0	67

Notes:

1. [7:1] bits indicate the slave address
2. LSB is a Read/Write indicator for Read/Write operation on a slave address
   a. LSB = 0 -> Write
   b. LSB = 1 -> Read
3. Refer Table 3 L, M, H values
   a. L = $V_{IL,TRILVL}$
   b. M = $V_{IM,TRILVL}$
   c. H = $V_{IH,\ TRILVL}$

Register Address

Table 17. Register Map Address

Register Address	Bit Range	Register name	Default	Type	SiT92313 Bit Name	Description and Function
0x00	7	OE_CTRL_0	0	RO	RESERVED	
	6:3		15	RW	SPARE0	
	2:0		0		SPARE	
0x01	7	OE_CTRL_1	1	RW	DIF2_ENABLE	Output Enable 0 : STOP_STATE Mode 1 : OE# Pin Control
	6		1		DIF1_ENABLE	
	5		1		DIF0_ENABLE	
	4:0		31		SPARE	
0x02	7:5	OE_CTRL_2	7	RW	SPARE	
	4		1		DIF7_ENABLE	Output Enable 0 : STOP_STATE Mode 1 : OE# Pin Control
	3		1		DIF6_ENABLE	
	2		1		DIF5_ENABLE	
	1		1		DIF4_ENABLE	
	0		1		DIF3_ENABLE	
0x03	7	OE_PIN_READ_BACK	0	RO	RB_OE7	OEb Pin Readback Register
	6		0		RB_OE6	
	5		0		RB_OE5	
	4		0		RB_OE4	
	3		0		RB_OE3	
	2		0		RB_OE2	
	1		0		RB_OE1	
	0		0		RB_OE0	
0x04	7:5	SBEN_PIN_READ_BACK	0	RO	RESERVED	
	4		1	RW	ACP_ENABLE	AUTOMATIC CLOCK PARKING
	3:1		0		SPARE	
	0		0	RO	RB_SBEN	SBEN Readback
0x05	7:4	VEN_REV_ID	0xa	RO	REVISION_ID	revA
	3:0		0x2		VENDOR_ID	SiTime product
0x06	7:0	DEV_ID	0	RO	DEVICE_ID	Device ID bits[7:0] map to register bits[7:0] directly.
0x07	7:5	BYTES_READ_COUNT	0	RO	RESERVED	
	4:0		7	RW	BYTES_READ_COUNT_VALUE	Writing to this register configures how many bytes will be read back on a block read.
0x08	7:0	OE_PIN_CONFIG_A_SBI_MASK_0	0	RW	SPARE	
0x09	7:0	OE_PIN_CONFIG_B_SBI_MASK_1	0	RW	SPARE	
0x0A	7:0	OE_PIN_CONFIG_C_SBI_MASK_2	0	RW	SPARE	

Register Address	Bit Range	Register name	Default	Type	SiT92313 Bit Name	Description and Function
0x0B	7:0	OUTPUT_IMPEDANCE_CONFIG_0	0	RW	SPARE	
0x0C	7:0	OUTPUT_IMPEDANCE_CONFIG_1	0	RW	SPARE	
0x0D	7:2	OUTPUT_IMPEDANCE_CONFIG_2	0	RW	SPARE	
	1:0		0		Z_CTRL_DIFF7	IMPEDANCE - 0: Nominal, 1: -5%(4'b0001), 2:+5%(4'b1111), 3:-10%(4'b0010)
0x0E	7	OUTPUT_IMPEDANCE_CONFIG_3	0	RW	SPARE2	
	6:5		0		Z_CTRL_DIFF6	IMPEDANCE - 0: Nominal, 1: -5%(4'b0001), 2:+5%(4'b1111), 3:-10%(4'b0010)
	4		0		SPARE1	
	3:2		0		Z_CTRL_DIFF5	IMPEDANCE - 0: Nominal, 1: -5%(4'b0001), 2:+5%(4'b1111), 3:-10%(4'b0010)
	1:0		0		SPARE0	
0x0F	7:6	OUTPUT_IMPEDANCE_CONFIG_4	0	RW	Z_CTRL_DIFF4	IMPEDANCE - 0: Nominal, 1: -5%(4'b0001), 2:+5%(4'b1111), 3:-10%(4'b0010)
	5		0		SPARE1	
	4:3		0		Z_CTRL_DIFF3	IMPEDANCE - 0: Nominal, 1: -5%(4'b0001), 2:+5%(4'b1111), 3:-10%(4'b0010)
	2		0		SPARE0	
	1:0		0		Z_CTRL_DIFF2	IMPEDANCE - 0: Nominal, 1: -5%(4'b0001), 2:+5%(4'b1111), 3:-10%(4'b0010)
0x10	7	OUTPUT_IMPEDANCE_CONFIG_5	0	RW	SPARE2	
	6:5		0		Z_CTRL_DIFF1	IMPEDANCE - 0: Nominal, 1: -5%(4'b0001), 2:+5%(4'b1111), 3:-10%(4'b0010)
	4		0		SPARE1	
	3:2		0		Z_CTRL_DIFF0	IMPEDANCE - 0: Nominal, 1: -5%(4'b0001), 2:+5%(4'b1111), 3:-10%(4'b0010)
	1:0		0		SPARE0	
0x11	7:0	OUTPUT_IMPEDANCE_CONFIG_6	0	RW	SPARE	
0x12	7:0	OUTPUT_IMPEDANCE_CONFIG_7	0	RW	SPARE	
0x14	7:4	STOP_STATE_CONFIG_REG	Refer note[3]	RW	OUTPUT_AMPLITUDE	The default amplitude is 0.8 Vpeak (typical). The typical step size is 25 mV, increasing monotonically from code 0 to code 15.
	3:2		0		SPARE	

Register Address	Bit Range	Register name	Default	Type	SiT92313 Bit Name	Description and Function
	1:0		0		STOP_STATE	0 : Low/Low 1 : HiZ/HiZ 2 : High/Low 3 : Low/High
0x15	7	INPUT_CONFIG_RB_LOSb_REG	0	RW	AC_IN	Enable receiver bias when CLKIN is AC coupled 0h = DC Coupled Input 1h = AC Coupled Input
	6		0		RX_TERM	Enable termination resistors on CLKIN1 0h = Input Termination R Disabled 1h = Input Termination R Enabled
	5		0		SPARE2	
	4		0	RO	CLK_ACQUIRED	A clock was acquired 1 = clock acquired
	3		0	RW	SPARE1	
	2		1		SDATA_TIMEOUT	Enable SMB SDATA time out monitoring 0h = Disable SDATA Time Out 1h = Enable SDATA Time Out
	1		0		SPARE0	
	0		0	RO	RB_LOSb	Real time read back of loss detect block output 0h = LOS Event Detected 1h = LOS Event Not-Detected
0x16	7:0	SBI_MASK_0	0	RW	SPARE	
0x17	7:0	SBI_MASK_1	0	RW	SPARE	
0x18	7:0	SBI_MASK_2	0	RW	SPARE	
0x21	7:0	SBI_DIFF_RB_0	255	RO	SPARE	
0x22	7:0	SBI_DIFF_RB_1	255	RO	SPARE	
0x23	7:4	SBI_DIFF_RB_2	0	RO	RESERVED	
	3:0		15	RO	SPARE	
0x26	7:1	NON_CLEARABLE_SMBUS_WRITE_LOCK	0	RO	RESERVED	
	0		0	RW	WRITE_LOCK	Non-clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can only be cleared by recycling power. 0h = SMBus Not locked for Writing 1h = SMBus Locked for Writing
0x27	7:2		0	RO	RESERVED	

Register Address	Bit Range	Register name	Default	Type	SiT92313 Bit Name	Description and Function
	1	LOS_NTY_N_CLEARABLE_SMBUS_WRITE_LOCK	0	W1C	LOS_EVT_NOTIFY	LOS Event Status. When high, indicates that a LOS event was detected. Can be cleared by writing a 1 to it. 0h = Not LOS Event Detected 1h = LOS Event Detected
	0		0	W1C	WRITE_LOCK_W1C	Clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written to. This bit can be cleared by writing a 1 to the bit. 0h = SMBus Not Locked for Writing 1h = SMBus locked for writing
0x66	7:4	RX_TERM_BUMP_REG	0	RO	RESERVED	
	3:0		0	RW	RX_TERM_BUMP	RX_TERM_BUMP : Rin Value(Ohms) 0 : 65.1 1 : 61.3 2 : 57.7 3 : 54.7 4 : 51.7 5 : 49.3 6 : 47.0 7 : 45.0 8 : 42.8 9 : 41.2 10 : 39.5 11 : 38.2 12 : 36.7 13 : 35.5 14 : 34.4 15 : 33.2
0x68	7:0	OE_PIN_CONFIG_A	255	RW	SPARE	
0x69	7:0	OE_PIN_CONFIG_B	0	RW	SPARE	
0x6A	7:0	OE_PIN_CONFIG_C	0	RW	SPARE	
0x6E	7:6	SLEW_RATE_CONFIG_0	0	RO	RESERVED	
	5:0		0	RW	SPARE	
0x6F	7:6	SLEW_RATE_CONFIG_1	0	RO	RESERVED	
	5:0		0	RW	SPARE	
0x70	7:6	SLEW_RATE_CONFIG_2	0	RO	RESERVED	
	5:0		0	RW	SPARE	
0x71	7:6	SLEW_RATE_CONFIG_3	0	RO	RESERVED	
	5:4		1	RW	SLEW_RATE_DIFF7	Refer Table 18
	3:0		0		SPARE	
0x72	7:6	SLEW_RATE_CONFIG_4	0	RO	RESERVED	
	5:4		1	RW	SLEW_RATE_DIFF5	Refer Table 18
	3:2		0		SPARE	
	1:0		1		SLEW_RATE_DIFF6	Refer Table 18

Register Address	Bit Range	Register name	Default	Type	SiT92313 Bit Name	Description and Function
0x73	7:6	SLEW_RATE_CONFIG_5	0	RO	RESERVED	
	5:4		1	RW	SLEW_RATE_DIFF3	Refer Table 18
	3:2		0		SPARE	
	1:0		1		SLEW_RATE_DIFF4	Refer Table 18
0x74	7:6	SLEW_RATE_CONFIG_6	0	RO	RESERVED	
	5:4		1	RW	SLEW_RATE_DIFF1	Refer Table 18
	3:2		0		SPARE	
	1:0		1		SLEW_RATE_DIFF2	Refer Table 18
0x75	7:6	SLEW_RATE_CONFIG_7	0	RO	RESERVED	
	5:2		0	RW	SPARE	
	1:0		1		SLEW_RATE_DIFF0	Refer Table 18
0x76	7:6	SLEW_RATE_CONFIG_8	0	RO	RESERVED	
	5:0		0	RW	SPARE	
0x77	7:6	SLEW_RATE_CONFIG_9	0	RO	RESERVED	
	5:0		0	RW	SPARE	

Notes:

1. Default values indicate the values of the bits set by power-up default.
2. RW - Read/Write, RO - Read Only
3. For changing the default amplitude value, Readback the amplitude code and apply the relative change

Table 18. Default Slew Code

Slew Code Reg. Individual Slew control.	Slew Rate V/ns @ for 0.8 V swing
0	3.8
1	2.9
2	2.5
3	1.8

Package Dimensions and Patterns

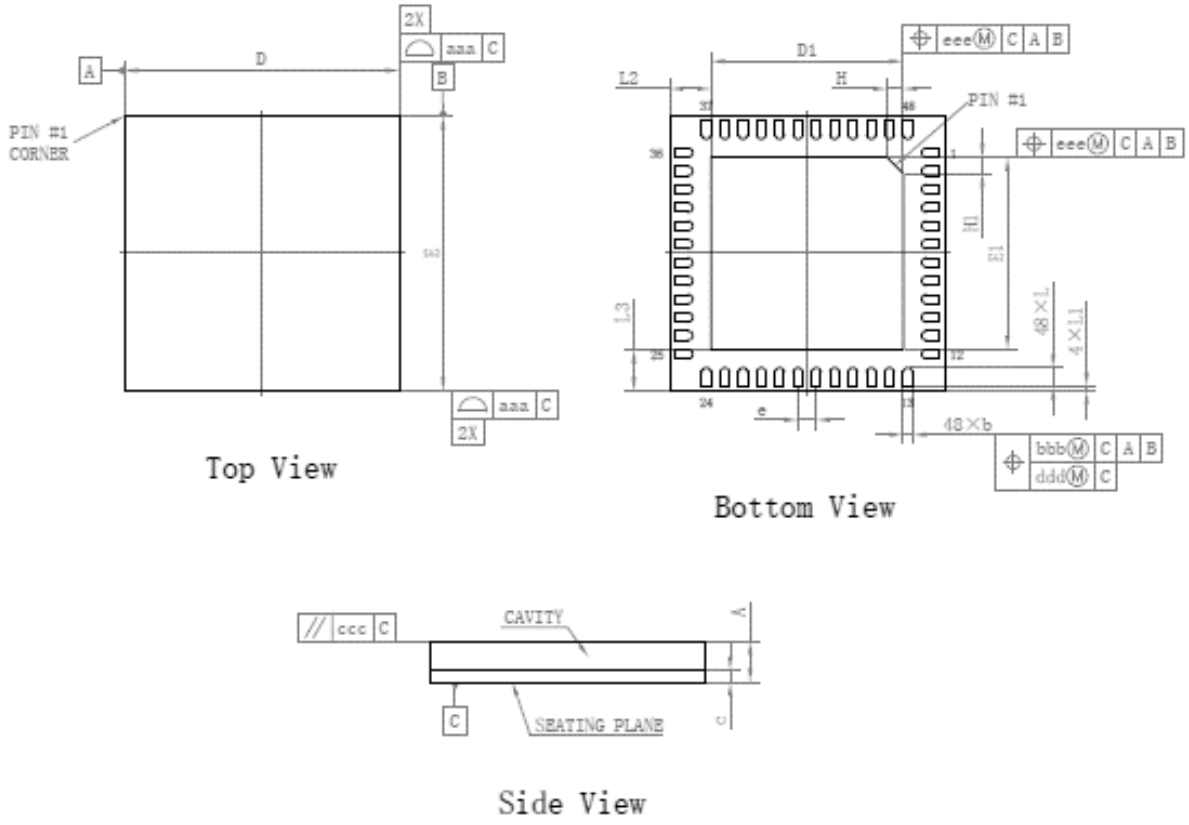


Figure 22. Package Diagram SiT92313 48 pin LGA

Symbol	Millimeter		
	MIN	NOM	MAX
A	0.800	0.900	1.000
c	0.210	0.250	0.290
D	5.900	6.000	6.10
E	5.900	6.000	6.10
D1	4.100	4.200	4.300
E1	4.100	4.200	4.300
H	-	0.350	-
H1	-	0.350	-
L	0.325	0.400	0.475
L1	0.025	0.100	0.175
L2	0.825	0.900	0.975
L3	0.825	0.900	0.975
e	-	0.400	-
b	0.150	0.200	0.250
aaa	0.100		
bbb	0.150		
ccc	0.100		
ddd	0.050		
eee	0.150		

Notes: All measurements are in millimetres(mm).

Land Pattern and Solder

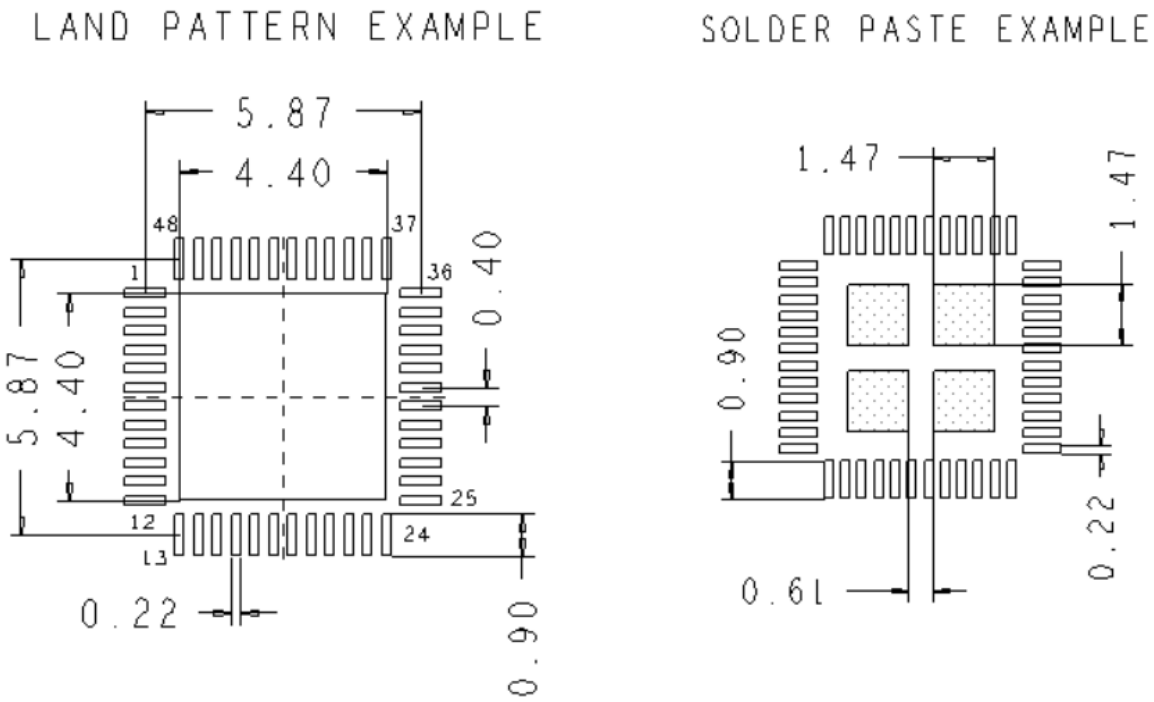


Figure 23. SiT92313 Land Pattern Diagram

General Notes:

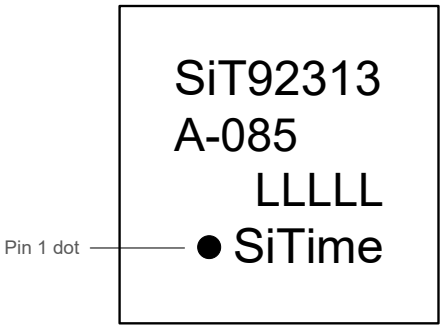
- All dimensions shown are in millimetres (mm) unless otherwise noted.
- This Land Pattern Design is based on the IPC-7351 guidelines.
- All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication allowance of 0.05 mm.

SOLDER MASK DESIGN:

- All metal pads are to be non-solder mask defined (NSMD).

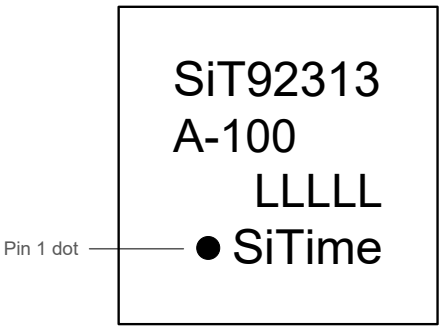
Top Marking

SiT92313 85 ohm output impedance device



Line 1: “SiT92313” SiTime part number
Line 2: “A-085” represent revision A and 85 Ohm impedance
Line 3: “LLLLL” Lot code from SiTime
Line 4: Pin 1 dot and “SiTime” logo

SiT92313 100 ohm output impedance device



Line 1: “SiT92313” SiTime part number
Line 2: “A-100” represent revision A and 100 Ohm impedance
Line 3: “LLLLL” Lot code from SiTime
Line 4: Pin 1 dot and “SiTime” logo

Revision History

Table 19. Revision History

Revisions	Release Date	Change Summary
0.5	7-Dec-2023	Initial Release
0.52	4-Apr-2025	Ordering Code for Packaging updated with 4Ku/reel code “P” and 500u/reel code “N” Added Top Marking section
0.55	21-Jan-2026	Updated Ordering Information, added 100 Ω option
0.56	25-Mar-2026	Datasheet tables have been updated to include support up to 105°C. Land pattern is added Additive jitter results with BRMC filter is added
0.57	11-Sep-2026	Updated for duction release
1.0	7-Oct-2026	Top marking and Ordering information updated Disclaimer updated

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439

© SiTime Corporation 2023-2026. The information contained herein is subject to change at any time without notice. SiTime assumes no responsibility or liability for any loss, damage or defect of a Product which is caused in whole or in part by (i) use of any circuitry other than circuitry embodied in a SiTime product, (ii) misuse or abuse including static discharge, neglect or accident, (iii) unauthorized modification or repairs which have been soldered or altered during assembly and are not capable of being tested by SiTime under its normal test conditions, or (iv) improper installation, storage, handling, warehousing or transportation, or (v) being subjected to unusual physical, thermal, or electrical stress.

Disclaimer: SiTime makes no warranty of any kind, express or implied, with regard to this material, and specifically disclaims any and all express or implied warranties, either in fact or by operation of law, statutory or otherwise, including the implied warranties of merchantability and fitness for use or a particular purpose, and any implied warranty arising from course of dealing or usage of trade, as well as any common-law duties relating to accuracy or lack of negligence, with respect to this material, any SiTime product and any product documentation.

HIGH RISK USE. BUYER UNDERSTANDS AND ACKNOWLEDGES THAT SELLER'S PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE AS COMPONENTS IN NUCLEAR FACILITIES. ADDITIONALLY, BUYER UNDERSTANDS AND ACKNOWLEDGES THAT, EXCEPT AS SET FORTH IN THE PARAGRAPH IMMEDIATELY BELOW, SELLER'S PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN LIFE OR CRITICAL SUPPORT DEVICES, DEFENSE, AEROSPACE, NAVIGATION, MEDICAL, OR OTHER MISSION-CRITICAL APPLICATIONS OR COMPONENTS WHERE HUMAN LIFE MAY BE AT STAKE. SELLER EXPRESSLY DISCLAIMS THE WARRANTIES SET FORTH ABOVE FOR ANY PRODUCT USES INCONSISTENT WITH THE TERMS OF THIS SECTION, AND BUYER SHALL DEFEND, INDEMNIFY AND HOLD SELLER HARMLESS FOR ALL LOSS, DAMAGE, EXPENSE OR LIABILITY IN CONNECTION WITH SUCH USES.

ENDURA® RUGGEDIZED PRODUCTS. ONLY SELLER'S ENDURA™ RUGGEDIZED PRODUCTS SHOULD BE CONSIDERED FOR LIFE OR CRITICAL SUPPORT DEVICES, DEFENSE, AEROSPACE, NAVIGATION, MEDICAL, OR OTHER MISSION-CRITICAL APPLICATIONS OR COMPONENTS WHERE HUMAN LIFE MAY BE INVOLVED OR AT STAKE.

SiTime owns all rights, title and interest to the intellectual property related to SiTime's products, including any software, firmware, copyright, patent, or trademark. The sale of SiTime products does not convey or imply any license under patent or other rights. SiTime retains the copyright and trademark rights in all documents, catalogs and plans supplied pursuant to or ancillary to the sale of products or services by SiTime. Unless otherwise agreed to in writing by SiTime, any reproduction, modification, translation, compilation, or representation of this material shall be strictly prohibited.